WHAT IS CLAIMED IS:

1. An error correction method for correcting an error event generated at one or more locations in received data by using a cyclic code, said error correction method comprising the steps of:

carrying out an exclusive-addition process of remainder data obtained as a result of dividing said received data by a generating function to remainder data obtained as a result of dividing data including an error event virtually generated in said received data by a generating function in order to find remainder data generated after a tentative-correction process for said virtually generated error event; and

correcting said error event of said tentative-correction process and an error event generated at a second location in said received data when said error event generated at said second location can be detected on the basis of said remainder data generated after said tentative-correction process.

2. An error correction method comprising the steps of:

carrying out a cyclic-replacement process on remainder data obtained as a result of dividing received data by a generating function in order to check whether or not a 1-event error is an event of an error to be corrected when generation of said 1-event error in said received data is detected on the basis of said remainder data;

if said 1-event error is determined to be an event of an error to be corrected, correcting said 1-event error in said received data on the basis of the number of times said cyclic-replacement process has been carried out and on the basis of said error event;

if said 1-event error is determined to be an event of an uncorrectable error, carrying out an exclusive-addition process of remainder data obtained as a result of dividing said received data by a generating function to remainder data obtained as a result of dividing data including an error event virtually generated in said received data by a generating function in order to find remainder data generated after a tentative-correction process for said virtually generated error event; and

correcting said error event of said tentative-correction process and an error event generated at a second location in said received data when said error event generated at

said second location can be detected on the basis of said remainder data generated after said tentative-correction process.

3. An error correction method according to claim 1 or 2, wherein a range of said tentative-correction process is specified by using reliability information obtained in a process to demodulate said received data.

4. An error correction circuit comprising:

a 1-event-error correction circuit for correcting a 1-event error of post-demodulation reproduced data; and

a 2-event-error correction circuit for receiving an output of said 1-event-error correction circuit and correcting a 2-event error, which cannot be corrected by said 1-event-error correction circuit.

5. An error correction circuit comprising:

a first linear feedback shift register for carrying out a cyclic-replacement process on remainder data obtained as a result of dividing received data by a generating function;

a second linear feedback shift register for receiving input data obtained as a result of said cyclic-replacement process carried out on remainder data obtained as a result of dividing data including an error event virtually generated in said received data by a generating function and for carrying out a cyclic-replacement process on said input data;

a multi-stage register for receiving data output by said second linear feedback shift register and sequentially transferring said data from stage to stage;

a plurality of exclusive-addition circuits for carrying out an exclusive-addition process of remainder data output by said first linear feedback shift register to each of outputs of said multi-stage register in order to virtually perform a tentative-correction process on said received data;

a plurality of third linear feedback shift registers each used for receiving each of said outputs of said exclusive-addition circuits and carrying out a cyclic-replacement process on said received outputs;

an error detection circuit for:

receiving remainder data obtained as a result of said cyclic-replacement process carried out by said first linear feedback shift register and checking said remainder data in order to determine whether or not a detected error can be corrected as a 1-event error;

if said detected error is determined to be correctable as a 1-event error, outputting a first error correction signal based on the number of times said cyclic-replacement process required for detection of said detected error has been carried out and based on an error event of said detected error in order to input remainder data obtained as a result of said cyclic-replacement process carried out by said third linear feedback shift registers and checking said remainder data in order to determine whether or not said detected error is an error event to be corrected; and

if said detected error is determined to be an error event to be corrected, outputting a second error correction signal based on the number of times said cyclic-replacement process required for detection of said detected error has been carried out and based on an error event completing said tentative-correction process; and

an error correction circuit for receiving said received date and, when said first and second error correction signals are received from said error detection circuit, correcting said received data.

6. An error correction circuit according to claim 5, wherein a range of said tentative-correction process carried out by said second linear feedback shift register and said multi-stage register is specified by using reliability information obtained in a process to demodulate said received data.

7. An information-recording/reproduction apparatus comprising:

a recording medium;

a head for recording data onto said recording medium and reproducing data from said recording medium;

a read/write channel for modulating data supplied to said head to be recorded by said head and demodulating a reproduced signal read out by said head;

a 1-event-error correction circuit for outputting data to be recorded obtained as a result of adding a cyclic code to data to be recorded onto said recording medium to said read/write channel and for correcting a 1-event error of reproduced data demodulated by said read/write channel;

a 2-event-error correction circuit for receiving an output of said 1-event-error correction circuit and correcting a 2-event error that cannot be corrected by said 1-event-error correction circuit;

a control circuit for receiving an output of said 2-event-error correction circuit and controlling a transfer of said output of said 2-event-error correction circuit to a host apparatus as reproduced data; and

a processor for controlling said recording medium, said head, said read/write channel, said 1-event-error correction circuit, said 2-event-error correction circuit and said control circuit.

8. An information-recording/reproduction apparatus comprising:

a recording medium;

a head for recording data onto said recording medium and reproducing data from said recording medium;

a read/write channel for modulating data supplied to said head to be recorded by said head and demodulating a reproduced signal read out by said head;

a first linear feedback shift register for providing said read/write channel with recording data obtained as a result of adding a cyclic code to data to be recorded onto said recording medium and for carrying out a cyclic-replacement process on remainder data obtained as a result of dividing reproduced data, which is received from said read/write channel after being demodulated by said read/write channel, by a generating function;

a second linear feedback shift register for receiving input data obtained as a result of said cyclic-replacement process carried out on remainder data obtained as a result of dividing data including an error event virtually generated in said reproduced data by a generating function and for carrying out a cyclic-replacement process on said input data;

a multi-stage register for receiving data output by said second linear feedback shift register and sequentially transferring said data from stage to stage;

a plurality of exclusive-addition circuits for carrying out an exclusive-addition process of remainder data output by said first linear feedback shift register to each of outputs of said multi-stage register in order to virtually perform a tentative-correction process on said received data;

a plurality of third linear feedback shift registers each used for receiving each of said outputs of said exclusive-addition circuits and carrying out a cyclic-replacement process on said received outputs;

an error detection circuit for:

receiving remainder data obtained as a result of said cyclic-replacement process carried out by said first linear feedback shift register and checking said remainder data in order to determine whether or not a detected error can be corrected as a 1-event error;

if said detected error is determined to be correctable as a 1-event error, outputting a first error correction signal based on the number of times said cyclic-replacement process required for detection of said detected error has been carried out and based on an error event of said detected error in order to input remainder data obtained as a result of said cyclic-replacement process carried out by said third linear feedback shift registers and checking said remainder data in order to determine whether or not said detected error is an error event to be corrected; and

if said detected error is determined to be an error event to be corrected, outputting a second error correction signal based on the number of times said cyclic-replacement process required for detection of said detected error has been carried out and based on an error event completing said tentative-correction process;

an error correction circuit for correcting said reproduced data when said first and second error correction signals are received from said error detection circuit;

a control circuit for receiving an output of said error correction circuit and controlling a transfer of said output of said error correction circuit to a host apparatus as reproduced data; and

a processor for controlling said recording medium, said head, said read/write channel, said first linear feedback shift register, said second linear feedback shift register, said

multi-stage register, said exclusive-addition circuits, said third linear feedback shift registers, said error detection circuit, said error correction circuit and said control circuit.

9. An information-recording/reproduction apparatus according to claim 8, wherein a range of said tentative-correction process carried out by said second linear feedback shift register and said multi-stage register is specified by using reliability information obtained in a process to demodulate said received data.